International Journal of Engineering Applied Sciences and Technology, 2022
Vol. 7, Issue 9, ISSN No. 2455-2143, Pages 90-96
Published Online January 2023 in IJEAST (http://www.ijeast.com)

DESIGN SPACE EXPLORATION OF LOW POWER FULL ADDER ACROSS MULTIPLE LOGIC STYLES AND PROCESS

Sparsha A.C, Sree Rekha K.P, Akshara S, B.P Harish
Department of Electronics and Communication Engineering
University Visvesvaraya College of Engineering, Bangalore University, Bangalore, INDIA

Abstract — **The signal processing in digital domain becoming ubiquitous, a full adder circuit module has gained prominence for its optimization in terms of its speed, power dissipation, noise margin and area. Further, with the advent of mobile applications on electronic devices, low power has emerged as an overriding design criterion. The proposed work aims to explore the design space of a low power full adder circuit and the implications of logic styles on power-delay trade-offs. Further, the issues impacting the selection of process for design for a given application are addressed. A 1-bit full adder circuit in static CMOS logic style and hybrid logic style is designed and optimized for low-power by carrying out exhaustive simulations using the LT spice simulator in 65 nm and 45 nm standard process to explore their power envelope, before low power process becomes necessary for design. Low power designs are demonstrated and the trade-offs with speed and area are explored.**

Keywords — **Design space exploration, Full adder, Static CMOS, PTL, Hybrid CMOS.**

I. INTRODUCTION

Signal processing in digital domain offers significant advantages like real-time processing, remote processing, and storage of signals. Digital signal processing is becoming ubiquitous, and it requires a series of additions and multiplications for processing. Hence, design of a full adder circuit, a versatile circuit module for addition and the basic processing element for multiplication, assumes significance. As such, an adder is a core element of any digital signal processor that determines its performance characteristics.

Further, with the advent of nanoscale integration, multimedia applications and convergence of communication and computing on mobile devices, low-voltage, low power circuit design has gained traction, in order to conserve the battery lifetime, with negligible or no speed penalty [1]-[4].

Full adder is a combinational circuit that adds 3 inputs, A, B and Carry input (Cin), to generate two outputs sum and carry output (Carry). The Boolean expressions of full adder are given by the Eq. (1) and Eq. (2).

$$\text{Carry} = A \cdot B + (A \oplus B)\,\text{Cin} \quad (1)$$

$$\text{Sum} = (A \oplus B) \oplus \text{Cin} \quad (2)$$

A low power full adder, in different logic styles, with minimum number of transistors is evaluated for delay, power and power-delay product (PDP) using 45 nm process. The post-layout Cadence Spectre simulation results showed a 20% to 30% power savings [5]. The effects of Variable Body Biasing (VBB) technique on full adders with transistor count of 28T, 20T, 16T, 14T, 11T and 10T are explored in a 90 nm design of 1-bit full adder cell. The results showed a peak power savings of 33% and average power savings of 13% against conventional bias [6]. To mitigate the logic swing issues usually seen in 10T full adder and to improve the speed of the carry bit, an improved 10T full adder is proposed. The post layout simulations in TSMC 0.35 µm CMOS process shows improved speed, low power consumption and reduced circuit complexity among peer 10T full adders [7]. An enhanced 10T full adder design implemented in 65 nm process is simulated and results showed an average power consumption of 2.94 µW and layout area savings of about 76.18% compared with 28T full adder design [8]. A 10T full adder in PTL logic style is simulated at 90 nm and 65 nm and the design is evaluated for power consumption and delay against the conventional 28T full adder for minimum PDP and the limitations of CMOS PTL on the designs, signal degradation and floating output node issues are explored [9],[10]. The performance of 8T and 10T full adder in PTL logic using logic level, circuit level and mixed mode implementation is evaluated post layout for power and area with minimum device count [11],[12]. In contrast, full adder circuits with minimum transistor size for low power and optimized device size for minimum PDP are investigated to demonstrate traditional CMOS and mirror topologies for optimal speed-power tradeoff [13].

In the proposed work, the design space of conventional 28T full adder in static CMOS logic style and a compact 10T full adder in hybrid logic style of static CMOS and pass transistor logic style are explored across 65 nm and 45 nm process for low power.

The remainder of the paper is organized as follows: Section II describes the simulation methodology for design space

International Journal of Engineering Applied Sciences and Technology, 2022
Vol. 7, Issue 9, ISSN No. 2455-2143, Pages 236-239
Published Online January 2023 in IJEAST (http://www.ijeast.com)

exploration across multiple logic style and process. While Section III describes the transient analysis of full adder, Section IV presents a detailed discussion on results. Section V concludes the work.

II. SIMULATION METHODOLOGY

The design objectives for the proposed design space exploration of low power full adder include low power consumption, glitch free output, signal integrity with no performance penalty. The 65 nm and 45 nm processes are considered as they are successive process generations with the high K metal gate (HKMG) technology being introduced at 45 nm. The low power objective is set with a standard 65 nm and 45 nm process to explore the power envelope of standard process, before low power process becomes essential for design. Further, static CMOS logic style and its combination with pass transistor logic referred to as hybrid logic style are considered as an additional dimension for design space exploration of the 28T and 10T 1-bit full adder cell, taken for illustration, respectively.

The 28T/10T full adder is simulated using LTspice simulator in 65 nm and 45 nm standard process. The rise time and fall time of input signals are set to 10 ps with a maximum frequency of 1 GHz. The transient analysis is performed to generate the Sum and Carry output and their high-to-low propagation delay τ_{pHL}, low-to-high propagation delay τ_{pLH} and average power dissipation are computed. While the propagation delays are computed as the time taken by the Sum/Carry output signal to make a transition from 10 % to 90 % for τ_{pLH} and 90 % to 10 % for τ_{pHL}, the average power dissipation is computed as the product of supply voltage VDD and the current drawn from the supply. The circuit area of the full adder is computed as the area occupied by all transistors, exclusive of interconnects.

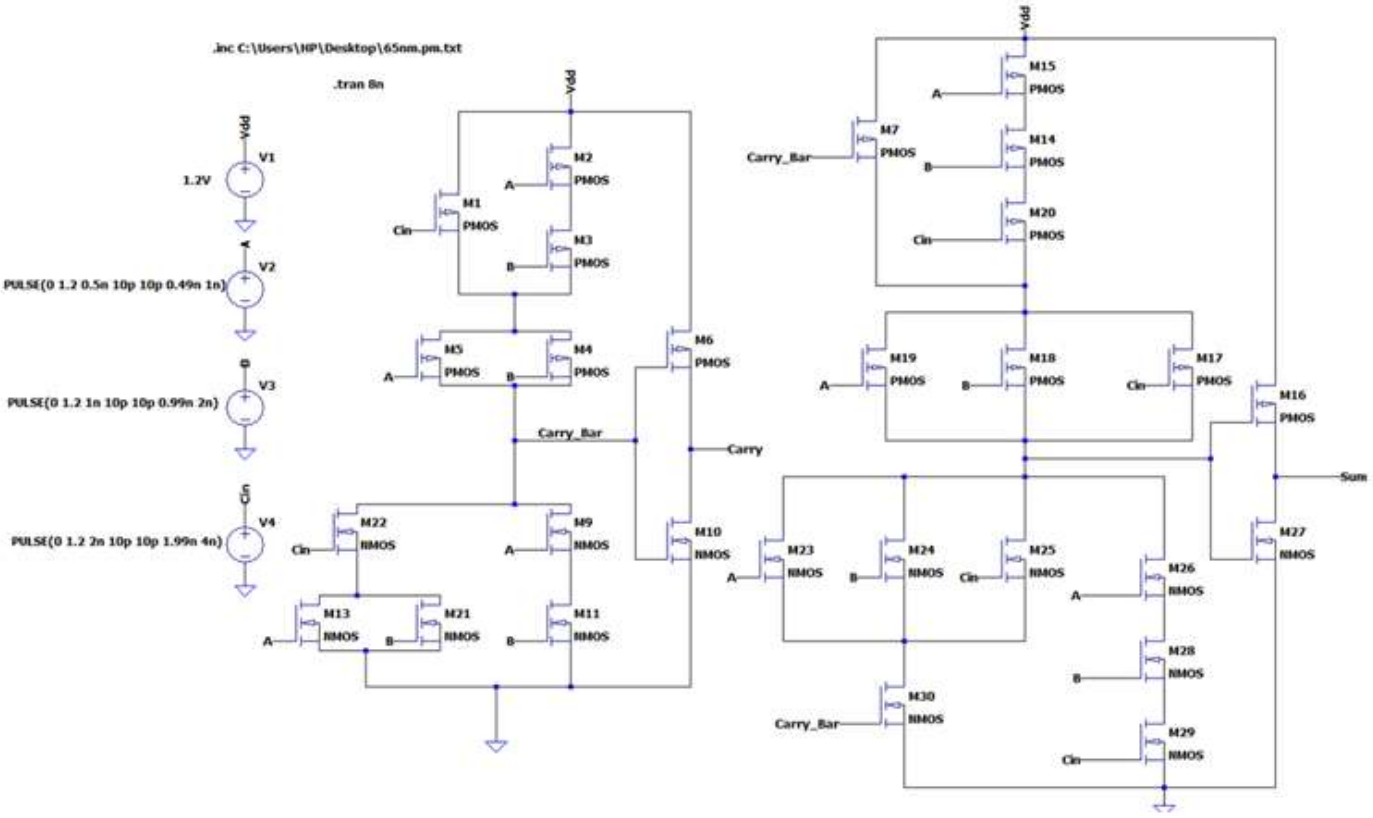

Fig. 1. 28T Full adder circuit in static CMOS logic

A. 28T Full Adder in Static CMOS Logic Style

The sum and carry output Eq. (1), (2) of the 1-bit full adder are rearranged as Eq. (3), (4) to yield 28T full adder cell.

$$Carry=(A\cdot B) +[Cin(A+B)] \quad (3)$$

$$Sum=(A\cdot B\cdot Cin) +[(A+B+Cin)\cdot Carry\_Bar] \quad (4)$$

The SPICE circuit schematic of 28T full adder in static CMOS logic style [14] is shown in Fig. 1. Static CMOS logic is indubitably the pre-eminent design family for its simplicity, rail-to-rail voltage swing, and low power consumption. However, the only drawback of static CMOS is its requirement for 2N transistors for a N-input logic.

B. 10T Full Adder in Hybrid CMOS Logic Style

To address the issue of large device count, Pass Transistor Logic (PTL) that allows the inputs to drive source and drain terminals in addition to the gate terminal is used to realize 1-bit

International Journal of Engineering Applied Sciences and Technology, 2022
Vol. 7, Issue 9, ISSN No. 2455-2143, Pages 236-239
Published Online January 2023 in IJEAST (http://www.ijeast.com)

full adder cell. The hybrid CMOS logic style is a combination of static CMOS logic and pass transistor logic. The sum and carry output Eq. (1), (2) of the 1-bit full adder are rearranged as Eq. (5), (6) to yield 10T full adder cell.

Carry=(A·B) + [Cin (A⊕ B)] (5)

Sum=Cin (A⊕ B)'+Cin'(A⊕ B) = (A⊕ B) ⊕ Cin (6)

To reduce the number of transistors utilized, multiplexer in pass transistor logic, shown in Fig. 2 is used to implement XOR logic as shown in Fig. 3. The truth table of 2:1 multiplexer configured as a XOR gate is given in Table 1.

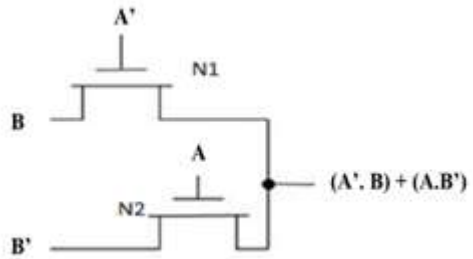

Fig. 1. MUX using pass transistor logic.

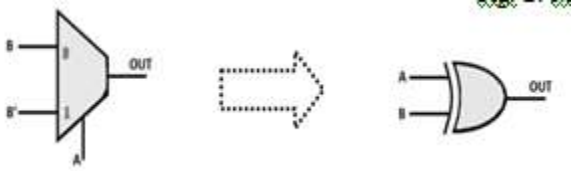

Fig. 3. Realizing XOR using 2:1 MUX

Table -1 Truth table of 2 input XOR gate using 2:1 MUX.

A	B	OUT	Observations
0	0	0	OUT = B
0	1	1	When A = 0
1	0	1	OUT = B'
1	1	0	When A = 1

The 1-bit full adder in hybrid CMOS logic style consists of 4 static CMOS transistors M1, M4, M2, M7 in combination with 6 PTL transistors M3, M8, M5, M9, M6, M10. The SPICE circuit schematic of 10T full adder in hybrid CMOS logic style [15] is shown in Fig. 4.

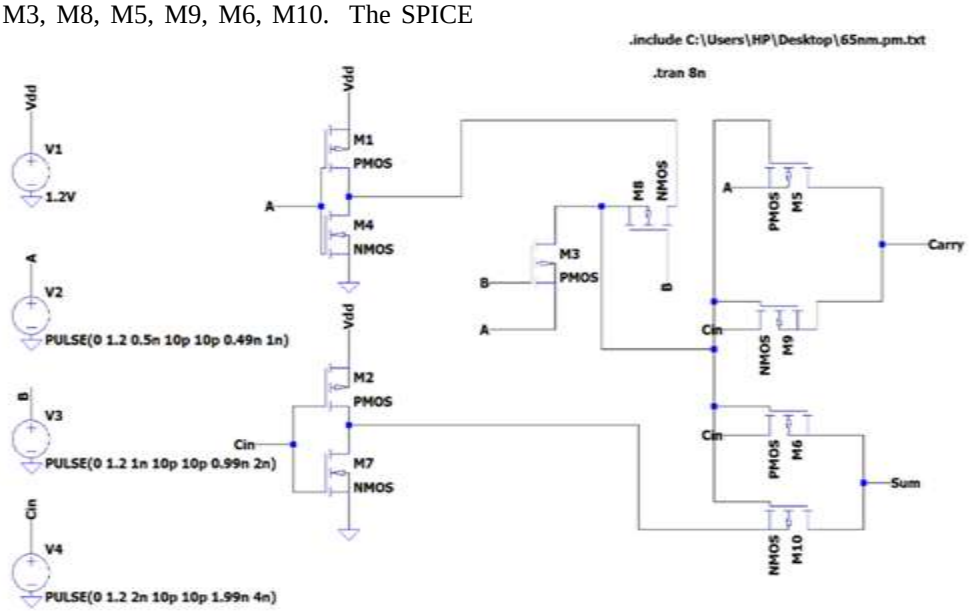

Fig. 4. 10T full adder circuit in hybrid logic style

International Journal of Engineering Applied Sciences and Technology, 2022
Vol. 7, Issue 9, ISSN No. 2455-2143, Pages 236-239
Published Online January 2023 in IJEAST (http://www.ijeast.com)

III. TRASIENT ANALYSIS OF FULL ADDER

The transient analysis of 28T full adder in static CMOS logic and 10T full adder in hybrid logic, in 65 nm and 45 nm process are carried out for delay computation. The transient response of 28T full adder in 65 nm is shown in Fig. 5 and in 45 nm is shown in Fig. 6. The transient response of 10T full adder in 65 nm is shown in Fig. 7 and in 45 nm is shown in Fig. 8.

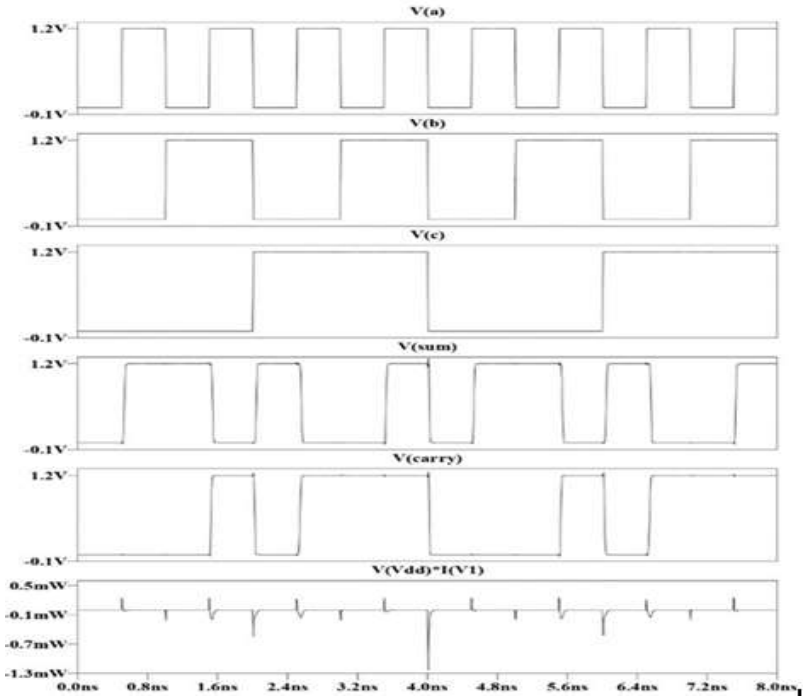

Fig. 5. Transient response of 28T full adder in 65 nm process

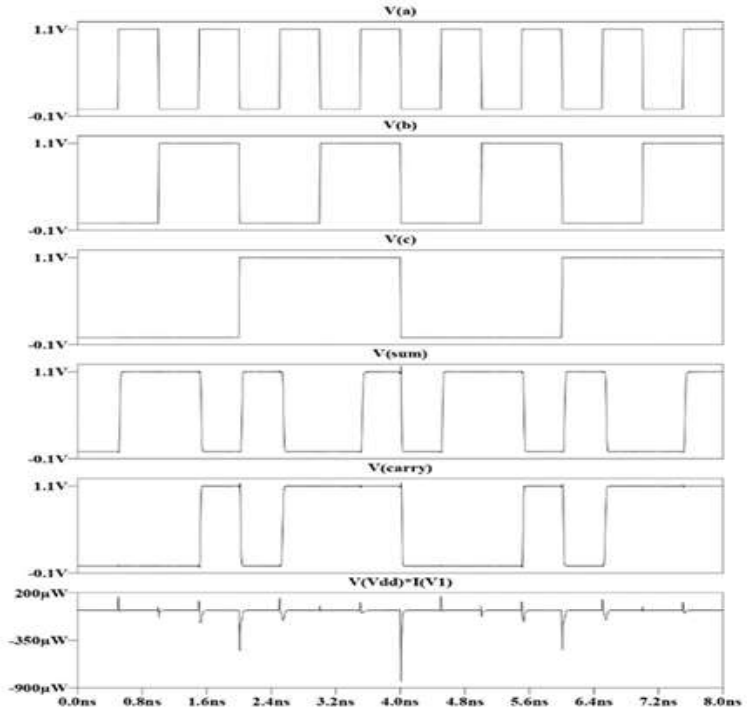

Fig. 6. Transient response of 28T full adder in 45 nm process

International Journal of Engineering Applied Sciences and Technology, 2022
Vol. 7, Issue 9, ISSN No. 2455-2143, Pages 236-239
Published Online January 2023 in IJEAST (http://www.ijeast.com)

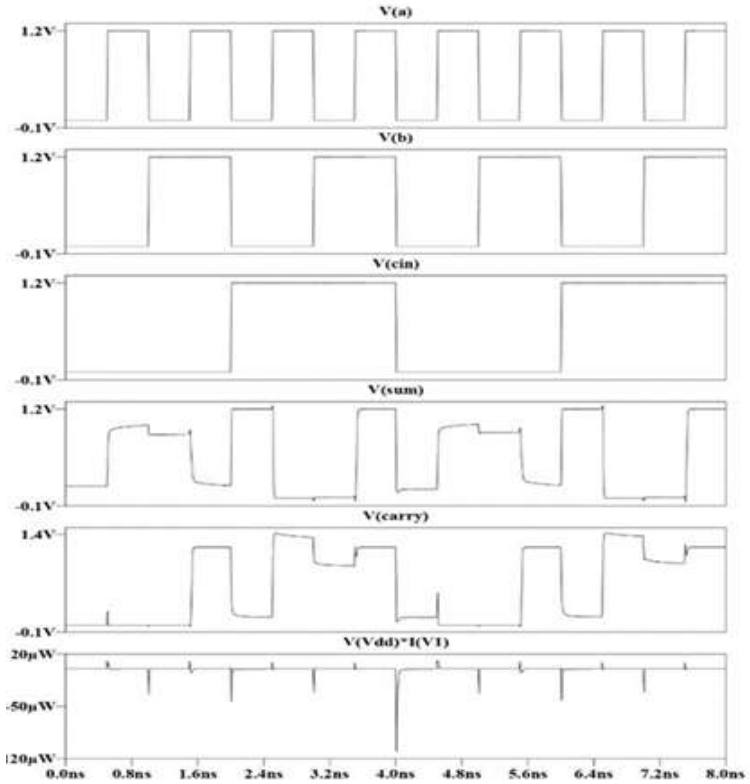

Fig. 7. Transient response of 10T full adder in 65 nm process

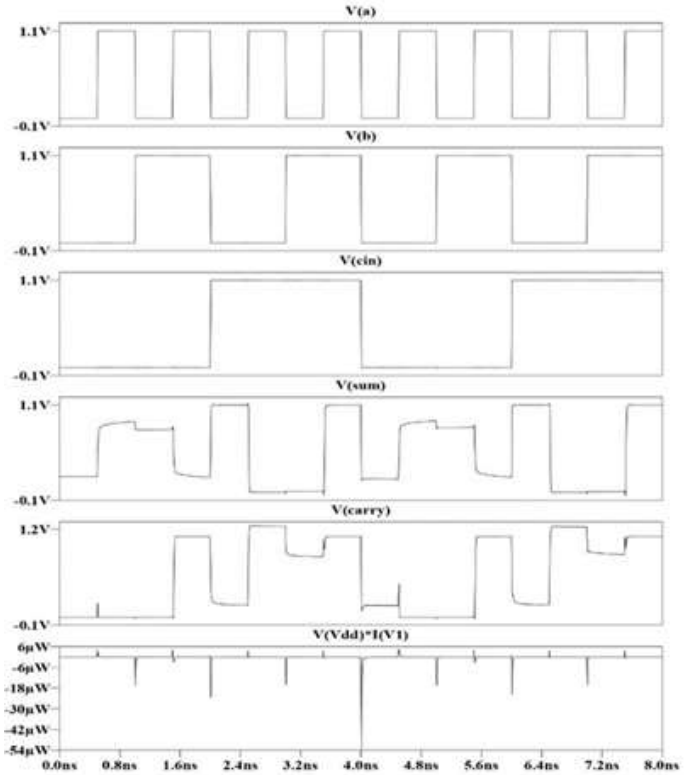

Fig. 8. Transient response of 10T full adder in 45 nm process

International Journal of Engineering Applied Sciences and Technology, 2022
Vol. 7, Issue 9, ISSN No. 2455-2143, Pages 236-239
Published Online January 2023 in IJEAST (http://www.ijeast.com)

IV. RESULTS AND DISCUSSION

The simulation results for delay, power dissipation and area of the 28T full adder and 10T full adder, in 65 nm and 45 nm process are tabulated in Table 2.

Table 2. Power-delay characterization of full adder in static CMOS and hybrid logic styles at 65 nm and 45 nm process.

Technology		65 nm		45 nm	
Transistor Count		Static CMOS 28T	Hybrid CMOS 10T	Static CMOS 28T	Hybrid CMOS 10T
Power Dissipation (µW)		7.984	0.505	5.55	0.246
Area (μm^2)		0.543	0.0861	0.327	0.0304
Sum Delay (ps)	τ_{pLH}	20.64	20.29	19.67	15.38
	τ_{pHL}	20.38	12.19	19.16	11.15
Carry Delay (ps)	τ_{pLH}	18.98	20.24	15.36	15.13
	τ_{pHL}	17.03	8.58	15.06	8.60

In 65 nm process, the power dissipation is 7.984 µW for 28T full adder and is 0.505 µW for 10T full adder, representing power savings of 16X, achieved by using hybrid logic style in place of static CMOS logic style. However, in 45 nm process, the power dissipation is 5.55 µW for 28T full adder and is 0.246 µW for 10T full adder, representing power savings of 22X, achieved by using hybrid logic style in place of static CMOS logic style. This demonstrates the significance of hybrid logic style over static CMOS logic style in achieving power savings of orders of magnitude. Further, the amount of power savings goes from 16X to 22X as design moves from 65 nm to 45 nm process.

The power dissipation of 28T static CMOS full adder is 7.984 µW in 65 nm process and is 5.55 µW in 45 nm, representing power savings of 30% across process. However, the power dissipation of 10T full adder in hybrid logic CMOS is 0.505 µW in 65 nm process and is 0.246 µW in 45 nm representing power savings of 51% across process. This demonstrates that hybrid CMOS logic style produces significant power savings, and the amount of savings increases with advancement in process.

The rising edge delay in generating the sum output, τ_{PLH} of 28T static CMOS full adder is 20.64 ps in 65 nm process and is 19.67 ps in 45 nm, representing a delay improvement by 5% and the corresponding falling edge delay, τ_{PHL} of 28T static CMOS full adder is 20.38 ps in 65 nm process and is 19.16 ps in 45 nm, representing a delay improvement by 6%. However, the rising edge delay in generating carry τ_{PLH} of 28T static CMOS full adder is 18.98 ps in 65 nm process and is 15.36 ps in 45 nm, representing a delay improvement by 19% and the corresponding falling edge delay τ_{PHL} of 28T static CMOS full adder is 17.03 ps in 65 nm process and is 15.06 ps in 45 nm, representing a delay improvement by 11%.

The rising edge delay in generating the sum output, τ_{PLH} of 10T hybrid logic CMOS full adder is 20.29 ps in 65 nm process and is 15.38 ps in 45 nm, representing a delay improvement by 24% and the corresponding falling edge delay, τ_{PHL} of 10T hybrid logic full adder is 12.19 ps in 65 nm process and is 11.15 ps in 45 nm, representing a delay improvement by 8%. However, the rising edge delay in generating carry τ_{PLH} of 10T full adder is 20.24 ps in 65 nm process and is 15.13 ps in 45 nm, representing a delay improvement by 25% and the corresponding falling edge delay τ_{PHL} is 8.58 ps in 65 nm process and is 8.60 ps in 45 nm, representing a marginal rise in delay by 0.2%.

The rising and falling edge delay in generating sum and carry of static CMOS full adder are fairly equal demonstrating symmetric rise time and fall time delays that are attributed to the static CMOS logic style. However, the rising and falling edge delay in generating sum and carry of 10T full adder in 65 nm and 45 nm process are not comparable because of the hybrid logic style used for the design of 10T full adder.

The area exclusive of interconnects, while for 28T full adder is 0.543 µm2 in 65 nm process and 0.327 µm2 in 45 nm process, for 10T full adder is 0.0861 µm2 in 65 nm process and 0.0304 µm2 in 45 nm process.

In summary, while the hybrid logic style CMOS offers small device count, low power with a speed penalty, the static CMOS logic style offers high speed with symmetrical rise and fall times with a corresponding power and area penalty.

V. CONCLUSION

A low-power 1-bit full adder cell in static CMOS logic style and hybrid CMOS logic style are designed and optimized for low power for mobile electronics applications. The simulated results show that the amount of power savings achieved with 10T FA in hybrid CMOS logic style against 28T FA in static CMOS logic is 16X in 65 nm process and is 22X in 45 nm process. The amount of power savings achieved in 45 nm process against 65 nm process is 30 % for 28T FA in static CMOS logic and 51 % for 10T FA in hybrid CMOS logic style. Hence, the hybrid CMOS logic style produces significant power savings, and the amount of savings increases with advancement in process. The low power designs with different logic styles and across process generations are implemented with marginal speed enhancements and no area penalty.

VI. REFERENCE

[1] Benjamin Franklin and T. Sasilatha (2019). "Design and Analysis of Low Power Full Adder for Portable and Wearable Applications", International Journal of Recent Technoklogy and Engineering (IJRTE), Vol. 7, No. 5S3 (pp. 295-299).

[2] Woo Wei Kai, Nabihah binti Ahmad and Mohamad Hairol Jabbar (2017). "Variable Body Biasing (VBB) based VLSI Design Approach to Reduce Static Power", International Journal of Electrical and Computer Engineering (IJECE), Vol. 7, No. 6 (pp. 3010-3019).

[3] Jin-Fa lin, Ming-Hwa Sheu and Yin-Tsung Hwang (2006). "Low-Power and Low-Complextly Full Adder Design for Wireless Base Band Application", Procedings of International Conference on Communications, Circuits and Systems, (pp. 2337-2341).

[4] V. J. Ylaya (2020). "Improved Design of Binary Full Adder", International Journal of Advanced Trends in Computer Science and Engineering, Vol. 9, No. 3 (pp. 4113-4116).

[5] Jan M. Rabaey, A. Chandrakasan and B. Nikolic (2003). "Digital Integrated Circuits: A Design Perspective", Pearson Education.

[6] H. A. Mahmoud and M. A. Bayoumi (1999). "A 10-Transistor Low-Power High-Speed Full Adder Cell", Proceedings of IEEE International Symposium on Circuits and Systems (pp. 43-46).

[7] Jin-Fa lin, Ming-Hwa Sheu and Yin-Tsung Hwang (2006). "Low-Power and Low-Complextly Full Adder Design for Wireless Base Band Application", Procedings of International Conference on Communications, Circuits and Systems (pp. 2337-2341).

[8] V. J. Ylaya (2020). "Improved Design of Binary Full Adder", International Journal of Advanced Trends in Computer Science and Engineering, Vol. 9, No. 3 (pp. 4113-4116).

[9] Kotthapalli Srujana, Kummari Shivani, Kuruva Thirumalesh & Lakku Yashaswi (2020). "Optimizing Conventional Full Adder Design for Power-Efficient Applications", Journal of VLSI and Computer systems, Vol. 7, Issue 10 (pp. 47-51).

[10] Sheetal Sahani & Dr. Bharti Chourasia (2020). "Design and Analysis of Low Power Consumption I0T-Full Adder Circuit", International Journal of Scientific Research & Engineering Trends, Vol. 6, Issue 5 (pp. 2790–2794).

[11] Palaniappan. T, Alwyn Rajiv S & Vidya P Janaki (2017). "Design and Analysis of Low Power Full Adder", International Journal of Advanced Research Trends in Engineering and Technology (IJARTET), Vol. 4, Special Issue 20 (pp. 73-77).

[12] Bappy Chandra Devnath & Satyendra N.Biswas (2019). "Low Power Full Adder Design Using PTM Transistor Model", Carpathian Journal of Electronic and Computer Engineering, Vol. 12, Issue 2 (pp. 15-20).

[13] Massimo Alioto & Gaetano Palumbo (2002). "Analysis and Comparison on Full Adder Block in Submicron Technology", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 10, No. 6 (pp. 806-823).

[14] Jan M. Rabaey, A. Chandrakasan and B. Nikolic (2003). "Digital Integrated Circuits: A Design Perspective", Pearson Education.

[15] H. A. Mahmoud and M. A. Bayoumi (1999). "A 10-Transistor Low-Power High-Speed Full Adder Cell", Proceedings of IEEE International Symposium on Circuits and Systems, (pp. 43-46).